IN THE CLAIMS

1. - 12. (Previously Canceled)

13. (Currently Amended) A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a plurality of N memory modules, wherein each of the memory modules includes:

a plurality M of memory devices, wherein each memory device internally contains a data in and a data out buffer, a column decoder and a row decoder;

a first register connected between the command and address bus and the plurality of memory devices, the first register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a second, data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the data in buffers of the plurality of memory devices for a write operation, the data register receiving and latching the data information from the data out buffers of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation;

a socket adapted to receive the memory module and to couple the memory module to the unidirectional command and address bus and to the bidirectional data bus; and

wherein a first load on the command and address bus is equal to N devices and a second load on the data bus is equal to N devices where the total number of memory devices is N*M.

14. (Previously Amended) The memory system according to claim 13 wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the first register of the memory module and a second delay introduced by the data register of the memory module.

15. (Original) The memory system according to claim 13 wherein each memory device is a dynamic random access memory device.

16. (Original) The memory system according to claim 13 wherein M equals 8.

17. - 31. (Previously Canceled)

32. (Previously Amended) A method of storing data in a pipelined memory system, wherein the pipelined memory system includes a memory module, a socket, and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder, and a row decoder, and wherein the socket couples the memory module to a unidirectional command and address bus and to a bidirectional data bus, the method comprising:

inserting the memory module in the socket;

communicating commands and addresses, through the socket to the memory module, on the unidirectional command and address bus;

communicating data, through the socket to the memory module, on the bidirectional data bus;

latching the commands and addresses in a first register;

latching the data in a data register;

driving the latched commands and addresses from the first register to the column and row decoders;

driving the latched data to the data in buffers; and

storing the data from the data in buffer in the addressable storage of one of the plurality of memory devices.

33. (Previously Amended) The method of claim 32, wherein communicating commands and addresses and communicating data includes executing a packet protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

34. (Previously Amended) A method of reading data in a pipelined memory system, wherein the pipelined memory system includes a memory module and a socket, wherein the socket couples the memory module to a unidirectional command and address bus and a bidirectional data bus, the method comprising:

inserting the memory module in the socket;

communicating commands and addresses, through the socket to the memory module, on the unidirectional command and address bus;

latching the commands and addresses in a first register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder;

communicating data from the addressable storage of one of the plurality of memory devices;

latching data in the data in and a data out buffer;

latching the data in a data register; and

communicating the data, through the socket to a memory controller, on the bidirectional data bus.

35. (Previously Amended) The method of claim 34, wherein communicating commands and addresses and receiving data includes executing a packet protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

36. (Previously Amended) A memory module comprising:

a data register;

a first register;

a plurality M of memory devices, wherein each memory device internally contains a data in and a data out buffer, and further contains a column decoder and a row decoder, wherein the data in buffer receives data information from the data register and wherein the column decoder and row decoder receive address information from the first register; and

a connector, wherein the connector includes command and address lines coupled to the first register and data lines coupled to the data register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus.

37. (Previously Amended) The memory module of claim 36, wherein the address information and the data information are communicated according to a packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

38. (Previously Added) The memory module of claim 36, wherein each memory device is a dynamic random access memory device.

39. (Previously Added) The memory module of claim 36, wherein M equals 8.

40. (Previously Amended) A method of storing data in a memory module having a connector, wherein the connector includes command and address lines coupled to a first register and data lines coupled to a data register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus, the method comprising:

coupling the connector to the socket;

receiving commands and addresses, through the command and address lines, from the unidirectional command and address bus;

receiving data, through the data lines, from the data bus;

latching the commands and addresses in the first register;

latching the data in a data register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage;

driving the latched data to the plurality of memory devices; and

storing the data in the addressable storage of one of the plurality of memory devices.

41. (Previously Amended) The method of claim 40, wherein the commands and addresses and the data is communicated according to a packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

42. (Previously Amended) A method of reading data in a memory module having a connector, wherein the connector includes command and address lines coupled to a first register and data lines coupled to a data register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus, the method comprising:

coupling the connector to the socket;

receiving commands and addresses, through the command and address lines, from the unidirectional command and address bus;

latching the commands and addresses in a first register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage;

reading data from the addressable storage of one of the plurality of memory devices;

latching the data in a data in and out buffer of the one of the plurality of memory devices;

latching the data from the data in and data out buffer in a data register associated with the plurality of memory devices; and

communicating the data from the data register, through the data lines, to the data bus.

43. (Previously Amended) The method of claim 42, wherein the commands and addresses and the data is communicated according to a packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

44. (Previously Amended) An electronic system comprising:

a microprocessor;

a memory controller coupled to the microprocessor;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a plurality of N memory modules, wherein each of the memory modules includes:

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer;

a first register connected between the command and address bus and the plurality of memory devices, the first register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the data in buffers of the plurality of memory devices for a write operation, the data register receiving and latching the data information from the data out buffers of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation;

a plurality of sockets adapted to receive the plurality of memory modules and to couple each memory module to the unidirectional command and address bus and to the bidirectional data bus; and

wherein each of the command and address bus and the data bus support N*M memory devices and only experience a load of N registers.

45. (Previously Amended) The electronic system of claim 44, wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the first register of the memory module and a second delay introduced by the data register of the memory module.

46. (Previously Added) The electronic system of claim 44, wherein each memory device is a dynamic random access memory device.

47. (Previously Added) The electronic system of claim 44, wherein M equals 8.

48. (Previously Amended) In an electronic system having a memory controller, a memory module, wherein the memory module includes a plurality of memory devices, and a socket, wherein the socket couples the memory module to a unidirectional command and address bus and a bidirectional data bus, a method of storing data in one of the plurality of memory devices comprising:

inserting the memory module in the socket;

communicating information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses to the unidirectional command and address bus;

communicating the commands and addresses from the unidirectional command and address bus, through the socket, to the memory module;

communicating data from the memory controller to the bidirectional data bus;

communicating the data from the bidirectional data bus to the memory module;

latching the commands and addresses in a first register;

latching the data in a data register;

driving the latched commands and addresses to the plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder;

driving the latched data to the data in buffers; and

storing the data in the addressable storage of one of the plurality of memory devices.

49. (Previously Amended) The method of claim 48, wherein communicating commands and addresses and communicating data includes executing a pipeline packet protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

50. (Previously Amended) In an electronic system having a memory controller, a memory module, wherein the memory module includes a plurality of memory devices, and a socket, wherein the socket couples the memory module to a unidirectional command and address bus and a bidirectional data bus, a method of reading data from one of the plurality of memory devices comprising:

inserting the memory module in the socket;

communicating information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses to the unidirectional command and address;

communicating the commands and addresses from the unidirectional command and address bus, through the socket, to the memory module;

latching the commands and addresses in a first register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder;

communicating data from the addressable storage of one of the plurality of memory devices;

latching the data in the data out buffer;

latching the data from the data out buffer in a data register; and

communicating the data, through the socket to the memory controller, on a bidirectional data bus.

51. (Previously Amended) The method of claim 50, wherein communicating commands and addresses and receiving data includes executing a pipeline packet protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

52. (Previously Amended) A memory system, comprising:

a unidirectional command and address bus in electrical communication with a memory control device;

a bidirectional data bus in electrical communication with the memory control device;

a plurality of N memory modules, wherein each of the memory modules includes:

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer;

a first register connected between the command and address bus and the plurality of memory devices, the first register receiving and latching commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching data information from the bidirectional data bus and driving the data information to the data in buffers of the plurality of memory devices for a write operation, the data register receiving and latching the data information from the data out buffers of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation;

a plurality of sockets adapted to receive the plurality of memory modules and to couple each memory module to the unidirectional command and address bus and to the bidirectional data bus; and

wherein each of the command and address bus and the data bus support N*M memory devices and only experience a load of N registers.

53. (Previously Amended) The memory system of claim 52, wherein the commands and addresses and the data information communicate using a pipelined packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

54. (Previously Added) The memory system of claim 52, wherein each memory device is a dynamic random access memory device.

55. (Previously Added) The memory system of claim 52, wherein M equals 8.

56. (Previously Added) A memory module having a plurality of pipelined memory subsystems, wherein each pipelined memory subsystem includes:

a first register;

a second register;

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer, a column decoder, and a row decoder, wherein the data in buffer receives data information from the first register and wherein the column decoder and row decoder receive address information from the second register; and

a connector, wherein the connector includes command and address lines coupled to the second register and data lines coupled to the first register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus.

57. (Previously Added) The memory module of claim 56, wherein the address information and the data information are communicated according to a packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the second register.

58. (Previously Added) The memory module of claim 56, wherein each memory device is a dynamic random access memory device.

59. (Previously Added) The memory module of claim 56, wherein M equals 8 and the number of memory subsystems equals two.

60. (Previously Added) The memory module of claim 56, wherein M equals 8 and the number of memory subsystems equals one.